

**ABSTRACT OF THE DISCLOSURE**

A calculation circuit for the division of a fixed-point input signal comprising a  
 sequence of digital data values having a width of  $n$  bits by an adjustable division factor  $2^a$   
 for the purpose of generating a divided fixed-point output signal, having a signal input (2)  
 for applying the data value sequence of the fixed-point input signal, a first addition circuit  
 (6), which adds the digital data value present at the signal input (2) to a data value buffer-  
 stored in a register (33) to form a digital first summation data value having a width of  
 $\max(n, a+1) + 1$  bits, a shift circuit (11) which shifts the first summation data value  
 present by  $a$  data bits toward the right, with the result that the  $\max(n, a+1) - a + 1$  more  
 significant data bits of the first summation data value are output at an output of the shift  
 circuit (11), a logic circuit (16), which, as a function of the sign of the first summation  
 data value, logically ANDs the  $a$  less significant data bits of the first summation data  
 value with a logic combination data value, or logically Ors them with the inverted logical  
 combination data value, and outputs them to the register (33) for buffer-storage of the  
 logically combined data value ( $d_{v1}, d_{v2}$ ), a second addition circuit (37), which, as a  
 function of the sign of the first summation data value adds the data value output by the  
 shift circuit (11) to a value one for eliminating the DC signal component to form a second  
 summation data value, and having a signal output for outputting the sequence of the  
 second summation data values as divided fixed-point output signal.